CADSTAR

Red-Hot PCB Design for Ice-Cool Multi-Gigabit Applications

TECHNICAL ARTICLE

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Abstract

Mass-market media-based applications generate an insatiable demand for faster upload and download. This demand is driving data communication speeds ever upward at all levels, including those that affect PCB design. Emerging SuperSpeed USB 3 hardware is capable of a dizzying 4.8 Gbit/s.

For all their relative merits, competing standards for ultra-fast signal transmission such as PCI Express, HyperTransport, USB 3 and FireWire have much in common at the level of PCB design requirements.

Perhaps surprisingly, the standardisation of signal transmission can even simplify PCB design, provided these crucial common denominators are properly considered. Even more surprisingly, there is often no need to increase power consumption to boost speed - in fact it can sometimes be reduced.

This article focuses on PCB design using built-in analysis tools, showing how the latest high-speed buses can be designed with the minimum hassle and maximum reliability.

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Requirements for New Hardware

New hardware typically has to be

- As fast as possible
- As low-power as possible
- Compliant with EMC (Electro-Magnetic Compatibility) regulations
- As small as possible

These requirements might seem to be in conflict, but let us consider how they can be addressed.

As Fast as Possible

Differential signalling is now the norm for carrying fast signals. Differential signal transmission using tightly-coupled parallel PCB tracks is more reliable than the single-ended variety. Complementary differential signals are controlled mainly by each other instead of by a separate ground plane. Technologies based on LVDS (Low Voltage Differential Signalling) are most commonly employed.

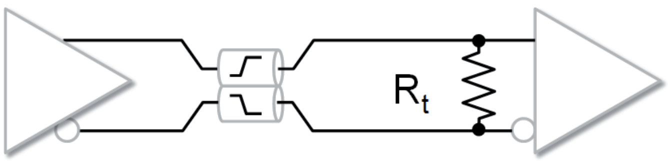

Figure 1: Point-to-Point Simplex
Point-to-point routing is becoming more common as it yields the highest bandwidth.

As Low-Power as Possible

Voltage swings should be minimized while maintaining noise immunity. Differential signals reject common-mode noise than is equal or near-equal on the + and – sides. By transmitting signals in a current loop with a differential termination, excess terminator power dissipation is avoided. Voltage levels are kept low, so overall power consumption is also low.

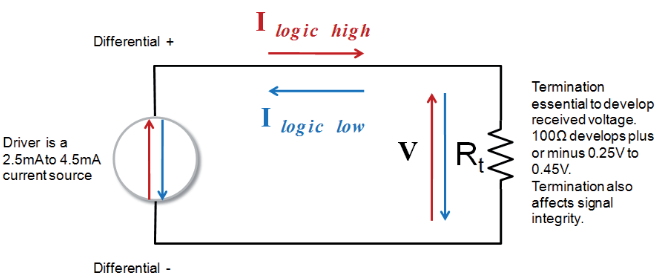

Figure 2: Current-Loop Signalling
In an LVDS differential signal, a small current is circulated through the far-end differential termination to develop a logic HIGH when current is circulated from Differential + to -, or a logic LOW voltage when the current is reversed.

Compliant with EMC Regulations

Compared to single-ended signals, differential signals with closely-coupled PCB tracks are both less susceptible to disturbance by radiated noise and lower emitters of EMI (Electro-Magnetic Interference) as shown by the simplified electric field lines shown in Figure 3 and Figure 4.

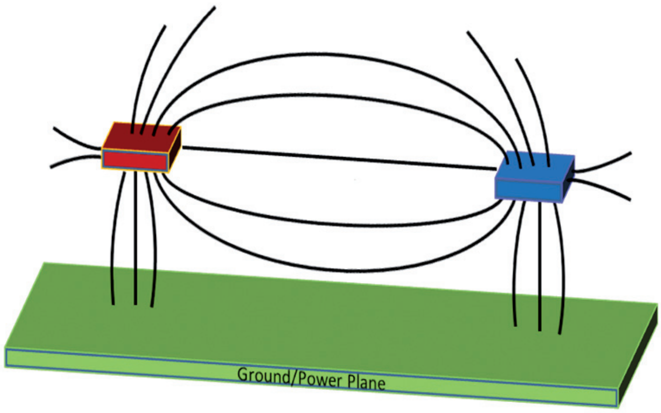

Figure 3: Differential Pair Routed on Outer PCB Layer
The electric field is mainly captured between the + and – sides of the pair and the ground/power plane.

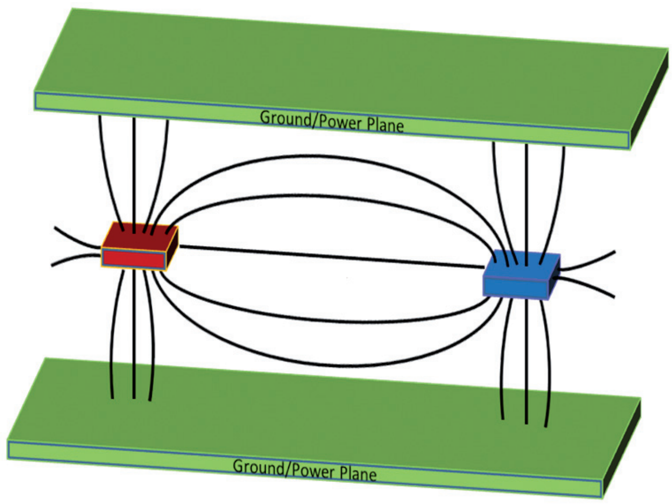

Figure 4: Differential Pair Routed Between Ground/Power Planes
The electric field is almost completely captured between the + and – sides of the pair and the ground/power planes above and below.

This localisation of fields, and the consequent benefits in EMC, are obtained only if the PCB routing keeps the + and – signals complementary over the entire route length, all the way from source to load. This cannot be guaranteed by length matching alone.

As Small as Possible

Higher bandwidth has traditionally consumed more PCB real estate, creating a conflict with the requirement for miniaturization.

In highway design, if it's not possible to build several standard roads linking two cities, the answer is to build one super highway.

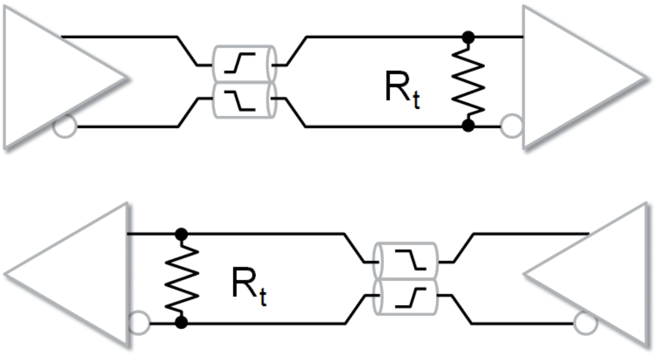

Figure 5: PCI Express Lane
Data and clock are combined and transmitted across Dual Simplex Lanes. Each differential pair has to be routed with precise symmetry, but controlling skew between different pairs is relatively low priority.

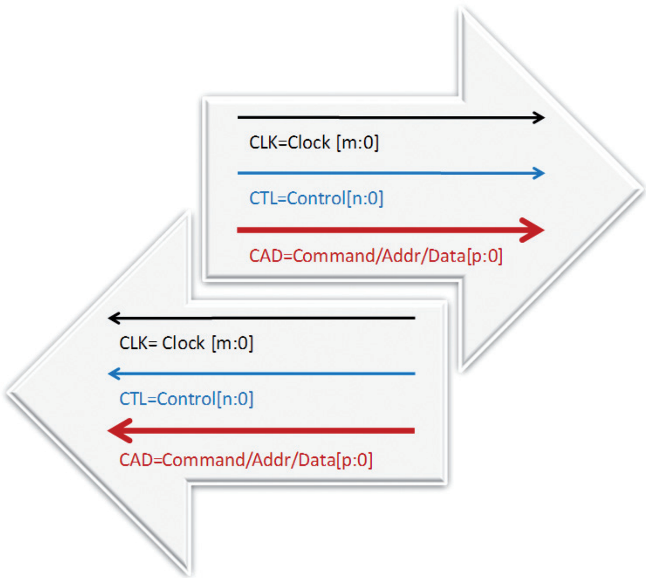

Figure 6: HyperTransport
The high-speed signals are also differential pairs routed point-to-point, and, as with PCI Express, require precise routing symmetry. In HyperTransport, however, tighter skew constraints are required between CAD, CTL and CLK pairs, since clock is transmitted separately from data. There is one clock for each link of up to eight bits of data.

Routing the Pairs

The lowest common denominator of all these fast buses is the need to route point-to-point differential pairs as symmetrically as possible. Each side must also be routed with symmetrical geometry, so that track widths, via types and via positions all match.

The routes must, as far as possible, stay at the spacing specified in the application notes, with only tiny variations.

A tall order indeed, but just as we don't expect to see unfilled frost holes and z-bends when driving on the expressway, so must our super-high-speed data channels be free of surprises.

Routing must be phase-matched; length matching alone is not sufficient. The route length from the driver to any point along the parallel-routed section must be kept equal within a very small tolerance.

Length differences that develop, for instance, due to route bends, must be compensated for as soon as possible after the point in the routing at which they arise.

Route width and parallel route spacing are defined in application notes for common layer stacks.

Many terminations are now on-die, so that no separate components are required, further simplifying routing.

Routing must not cross gaps in power or ground planes above or below.

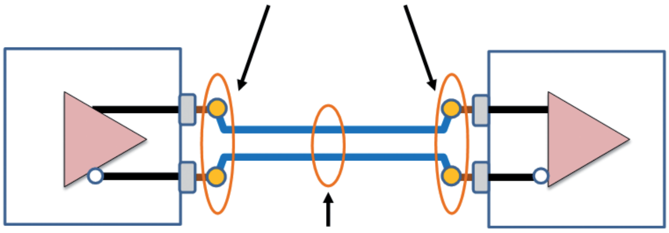

Figure 7: Routing a Differential Pair
Differences between differential pair routes must be kept within precise, small tolerances.

High-end PCB layout applications offer various solutions to this routing problem; for instance in the Zuken P.R.Editor 5000HS add-on to the CADSTAR suite, the most effective solution is to use semi-automatic Trunk Routing, where the pair is routed to constraints as a single item. Routing is kept balanced, except for small corrections, with the benefit of on-cursor, real-time visibility.

Analysis

The most valuable analysis is often performed before the start of physical design, by investigating design scenarios. The change from parallel single-ended to differential serial signalling for major data buses makes a big difference to the relative importance of various board and etch features.

In single-ended signalling, most significant electromagnetic coupling is between the PCB track and ground or power planes above or below.

In differential signalling with closely-coupled, parallel tracks, there is significant electromagnetic between the tracks, as illustrated in Figure 3 and Figure 4.

PCI Express, for instance, is designed to be implemented on low-cost PCB layer stacks, including four-layer FR-4, where routing is on surface layers.

Although surface layers are typically etched at a copper weight of half an ounce, giving etched copper thickness of 18 microns, subsequent plating processes often increase that to around 48 microns. Variations in etching and plating also combine to make the cross-section shape diverge from its ideal rectangular form.

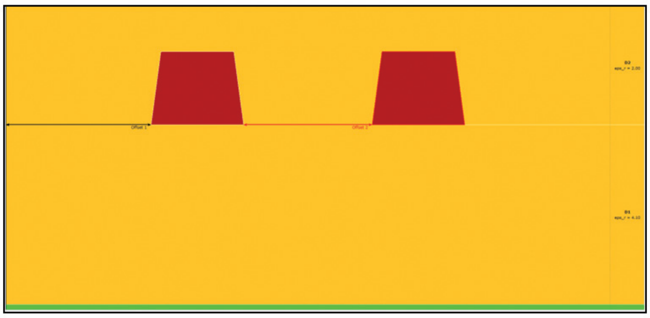

Figure 8: Cross-Section of Differential Pair Tracks Analyzed within Zuken SI Verify
Thickness and cross-section shape are highly significant for closely-coupled differential pairs.

The cross-section shown in Figure 8 yields calculated Odd Mode impedance of 48.5Ω, meaning the ideal differential termination would be 99Ω (double the odd-mode impedance).

If, however, we ignore plating, and assumed the track cross-section to be rectangular, the Odd Mode impedance becomes 51Ω, and the predicted ideal termination 102Ω.

High-speed serial signals often use line codes such as 8-10 bit encoding to optimize the digital signal for transmission. 8-10 bit encoding maps 8-bit symbols to 10-bit symbols. By achieving near-balance of ones and zeros, the mean DC level is balanced around its centre so that capacitive AC terminations work effectively.

The line should be simulated to create an eye pattern with the chosen line code and expected jitter level, as shown in Figure 9, so its performance can be assessed early in the design phase.

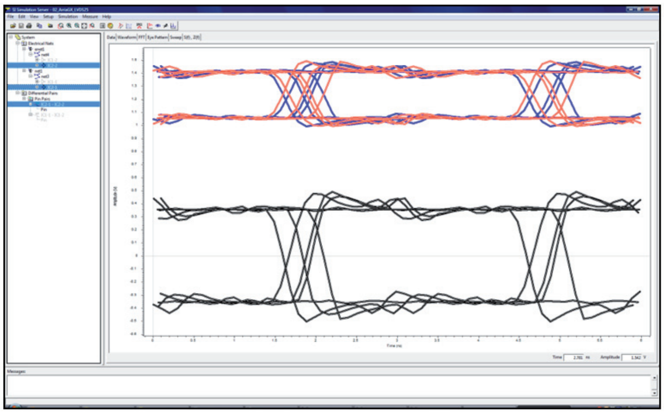

Figure 9: Eye Pattern for LVDS Point-to-Point Connection Analyzed within Zuken CR-5000 Lightning
Eye patterns are generated for both the separate differential + and – inputs (top) and the resultant differential received signal (bottom).

Conclusion

For the most common PCB form factors, latest signal transmission technologies are designed to tolerate significant variations in manufacturing processes, provided physical features are consistent within each PCB, and symmetrical where required. Relatively-generous tolerances are particularly useful now that much manufacturing is outsourced.

Accurate prediction of electrical behaviour is still required, not only for niche products, but within the mainstream. This ensures maximum reliability in the face of unexpected environmental and process variations, and facilitates later design changes and upgrades.

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