



High-Speed Digital Design with CADSTAR SI Verify and P.R.Editor

W H I T E P A P E R

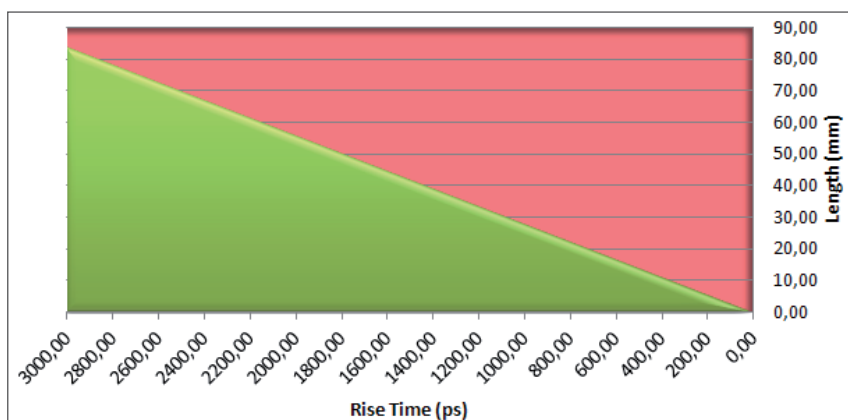
Plan and Verify your PCB Design for Right-The First-Time Signal Integrity

If you do not consider signal integrity in high-speed digital or part-digital PCB design, your prototype will probably not work or will work unreliably.

So is your design high-speed? This is where things may not be as they first appear. Many new PCBs include circuits that are clearly high-speed, such as PCI Express (PCIe) and USB3 SuperSpeed buses running at several GHz.

Double Data Rate (DDR, DDR2, DDR3) memory has become a standard part of many designs; if you use these memory chips it does not matter how fast you clock them – your PCB becomes high-speed in all cases. The key to knowing whether you need to worry about signal integrity is not the frequency but the output transition times: how long it takes digital signals to go from low to high or high to low.

This chart shows the approximate trace length at which signal integrity becomes a concern for a given transition time. When the propagation time – the time for a signal to travel along the trace - is half the rise time or more, major signal integrity issues affect even point-to-point routing. Less well-known is the fact that routing topology for multidrop/multipoint signals such as data and address buses starts to affect signal integrity much earlier, when the propagation time is one sixth of the rise/fall time.



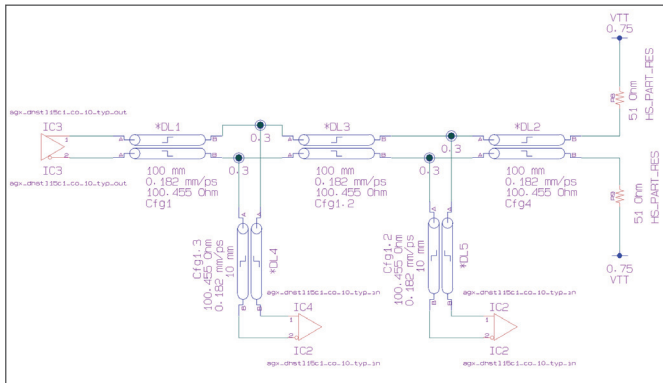
In DDR2 memory and many FPGA signals, rise/fall times can be in the order of 200ps, so that even at 6mm trace length, you must consider Signal Integrity.

Planning Signal Integrity from the Outset

With SI Verify you can approach signal integrity systematically. Before committing physical board design, it is easy to check whether you have the right layer stack and whether the topology you have in mind will give good results.

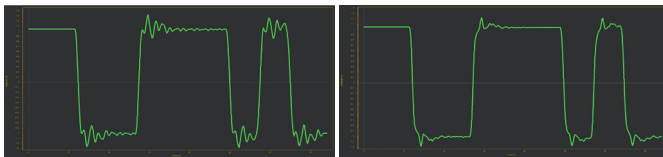
Say you are designing a 1.5V differential signal running from an FPGA to two receivers.

With a few clicks you set up a scenario representing the proposed topology, including vias and differential traces. Notice the 10mm stub traces that connect to the two receivers.



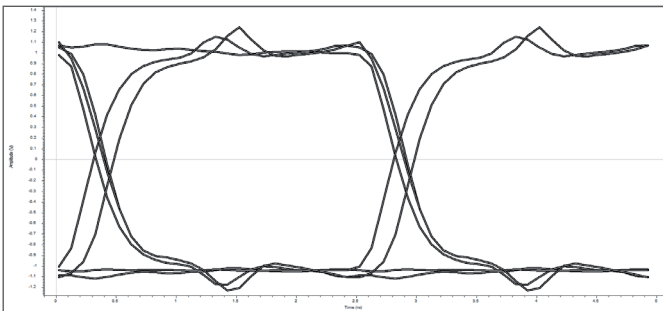
Long stubs can distort signals

The simulated waveform (left) is far from satisfactory, showing considerable distortion, so this signal will not operate as reliably as it should. So you change the scenario so that the differential pair is routed on a single layer with minimal or no stubs. The new waveform (right) is now much smoother, and an eye pattern analysis with 2 percent injected jitter confirms by its large eye opening that the proposed topology will yield improved reliability.



Distortion is visible at the receiver

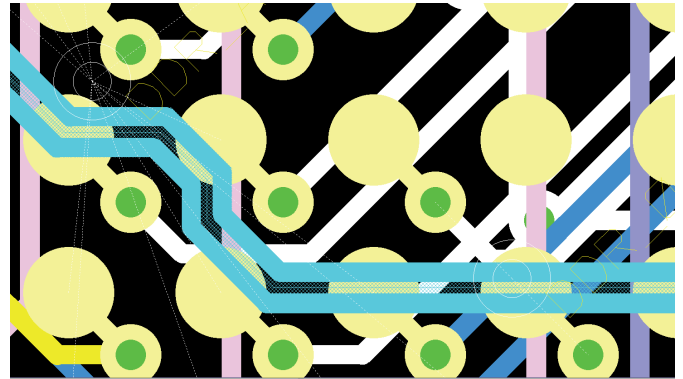
With improved routing topology the signal is much smoother



Eye patterns predict the reliability of high-speed signal transmission

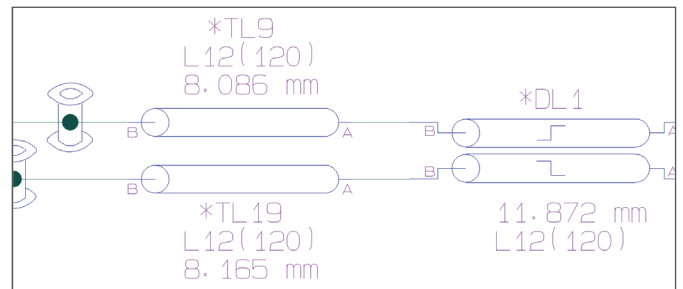
Confirming Results

Once you have routed a section of your design, you can, with just a mouse click, extract the equivalent circuit into exactly the same tool you used to plan your topology, and then simulate in exactly the same way. This is a section of the physical routing, completed using P.R.Editor 5000HS.



Important design detail is extracted for analysis

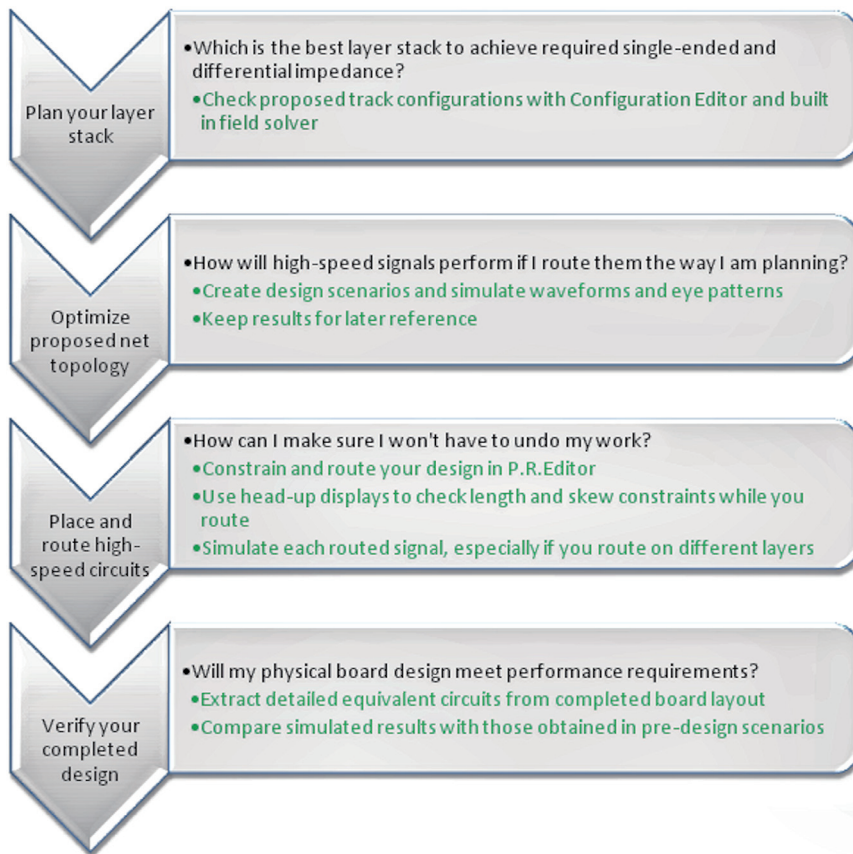
All significant design details are extracted, including electromagnetic coupling, layer-to-layer equivalent circuits for vias and coupling to power/ground tracks and areas on multiple layers. This means simulation takes into account even subtle effects on signal integrity.



Physical design data is converted into an equivalent circuit

The beauty of this approach is that you need learn only one simulation technique and one user interface. When different methods are used at different design stages, it is all too easy to mistake a consistency issue for a difference in results. With SI Verify, consistency is guaranteed because there is no change at all in the simulation or modelling environment. Furthermore, all of these capabilities are available within the same user interface, shared by SI Verify and advanced placement and routing environment P.R.Editor 5000HS. The two tools are available separately or as a combined package.

Typical Design Sequence



Conclusion

Signalling standards for high-speed buses using SSTL, HSTL, LVDS and other popular technologies have helped rationalize the design process by improving compatibility between hardware. Frequencies go higher while schedules get shorter. Device vendors now include smart distortion-countering technology for into their high-end devices, but even with the help of these hardware features, full-flow consideration of signal integrity is essential.

By employing a structured approach as outlined in this whitepaper, you can design boards featuring popular high-speed signalling standards, as well as more mature high-speed logic families, with maximum confidence.